Comparison of Different OVRT Test Benches in the Context of Realistic Over-Voltage Events

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***Abstract*—The ability of generators to ride through over-voltages has become increasingly important in recent years. The research project *OVRTuere* (FKZ 0350041) investigates whether existing HVRT (high-voltage ride-through) requirements represent the most cost-effective solution. It also deals with the verification of the HVRT-capability of generators by means of testing. This includes the comparison of the capabilities of different test facilities, such as temporary over-voltage magnitudes, voltage phase shifts and transients at the beginning and end of disturbances. This paper gives an overview of six types of HVRT test facilities. It provides an initial comparison of the facilities in terms of sub-cycle transients after beginning and end of disturbances.**

***Index Terms*—fault ride through, grid fault, over-voltages ride through, test benches, grid code testing**

I. Introduction

With the increasing complexity of the electrical transmission and distribution grids, the expectations for the grid-friendly behaviour of grid-connected generators and energy storage systems are rising. In the past, the expected reaction to grid disturbances has concentrated solely on under-voltage events (under-voltage ride-through, UVRT), whereas recently many international grid connection guidelines have included over-voltage testing (over-voltage ride-through, OVRT) [1]. Different types of test benches are available for testing the OVRT capabilities. These can vary greatly in terms of transient events, voltage ramps or impedance changes during the simulated fault. Since especially power electronic devices like inverters are very sensitive to transient voltage changes, it is important to analyse which test bench can simulate the most realistic over-voltage events. In the following, six test benches for OVRT tests are presented and their functionality is explained. The transient behaviour of the test benches during no-load tests is shown on the basis of the fault occurrence and fault end, showing plotted data from real measurement campaigns.

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II. Over-voltage events in interconnected power systems

An temporary over-voltage event is given when the voltage is above 1.1 pu for a period of 0.02 s to 3600 s [2]. Over-voltages that are shorter than 0.02 s are classified as transient. Depending on the corresponding voltage level, generation systems must withstand over-voltages for different durations [3].Temporary over-voltages can occur for variety of reasons, such as phase-to-earth faults in systems that are not solidly earthed or the energisation of transmission lines. In transmission grids, an important cause of over-voltages is the sudden de-loading of the highly loaded grids. This can be observed especially with a high percentage of wind turbine generators (WTG) in the system [4]. High active power transfers lead to a high "consumption" of reactive power (I^2X). During a fault in the transmission system, WTGs reduce their active power output to support the voltage through the injection of reactive current. When the fault is cleared, the active power output of the WTGs may initially be very low and may take up to a second (in some cases even more) to increase to the pre-fault level. The temporary reduction in the active current after fault clearance, compared to the pre-fault condition, causes a reduction in the reactive power consumption. This may cause the voltages to rise compared to pre-fault values, potentially causing generators to trip, thereby jeopardising system security. In some cases, Static Synchronous Compensators (STATCOM) or other equipment has been installed to counteract the temporary over-voltages [4]. In 2012 over-voltages in the German transmission system were observed following the clearance of a two-phase fault on a transmission line. Generation losses occurred due to the inability of some generators to ride through low and/or high voltages, amounting to almost 1.7 GW in total [1]. In North China, large-scale tripping of WTG occurred during an event in 2012 due to the inability of the generators to ride through over-voltages [5]. The relevance of over-voltages events increases with higher power transfers and a higher penetration of WTGs. The slower the active power recovery after a fault, the higher the duration of over-voltages. The effects of temporary over-voltages need to be managed to assure the stability and security of the power system. This may include the installation of devices that limit over-voltages and ensuring that generators are capable of riding through expected disturbances.

III. Description of the analyzed test benches

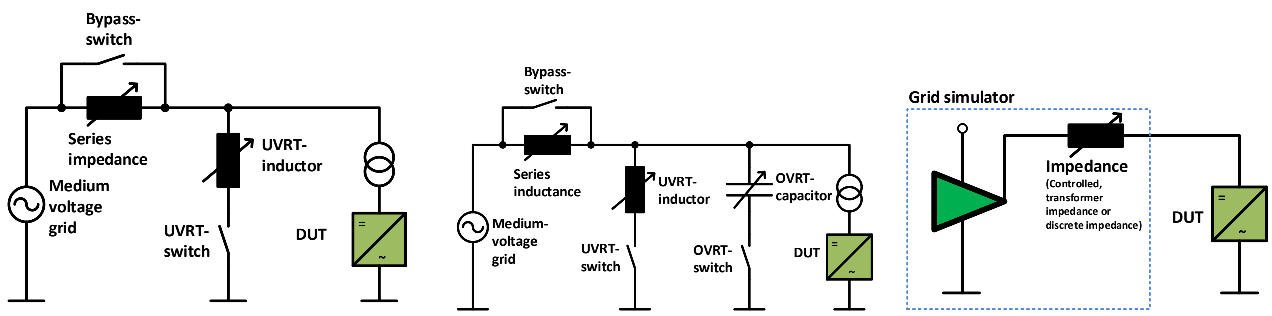
In this paper the test facilities listed below and shown in Figure 1 are compared to each other. All the test benches are able to create temporary over-voltages at the connections terminals of a device under test. The working principles and main features of these six approaches are explained below.

A. *Inverted inductive UVRT test bench*

The inverted inductive UVRT test bench makes use of a commonly used under-voltage ride through (UVRT) test, which are based on the inductive voltage-devider concept [6, S. 207-208]. The single-line diagram is shown in figure 1a. In order to use this UVRT test bench to generate OVRT events, a device-under-test (DUT) transformer is required that can be adjusted to the desired over-voltage level, e.g. 115% of nominal voltage. Then the voltage of the DUT is reduced to 100% of nominal voltage by activating test circuit (bypass switch open / UVRT switch closed). Subsequently the DUT will then be started and set to the desired operational point. In this stage the over-voltage fault event can be created by opening the UVRT-switch, which results in an sudden step to the voltage level adjusted before. The fault situation is stopped by closing the UVRT switch again. The test setup generally enables symmetric faults as well as 2-phase and 1-phase faults. One drawback of this test setup is, that the parallel inductor is energized with high currents for a rather long period of time (range of few minutes). This leads to a significant heating of the inductors. The resulting cooling times are a major limitation of the repetition rate when performing measurement campaigns.

B. *LC-resonant tank*

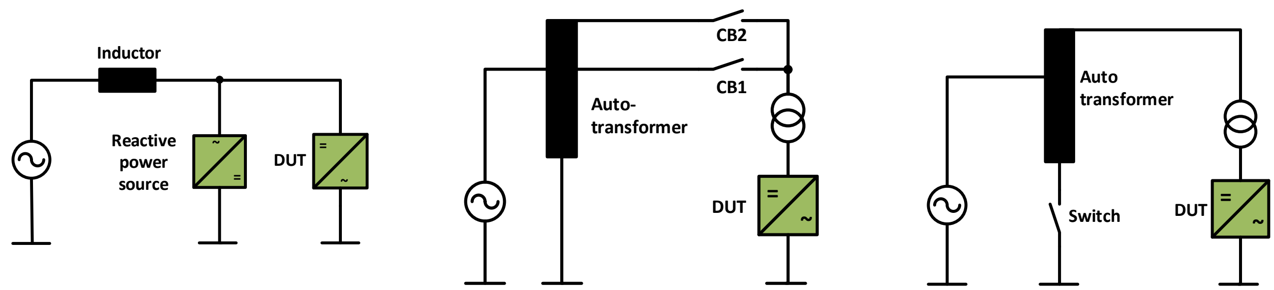
The LC-resonant tank adds a capacitor to the well-known UVRT-test setup in order to form a series LC-resonant circuit, as can be seen in figure 1b. Before the fault, the series impedance bypass is closed and the UVRT and OVRT switches are open. By closing the OVRT switch, the capacitors are energized. By opening the bypass switch, the OVRT event is initiated, since the now-active inductor is forming a LC-resonant circuit with the capacitor. By closing the bypass switch again, the DUT voltage returns to nominal voltage. The setup is capable of producing OVRTs and UVRTs. Faults can be on 3 phases, 2 phases and on 1 phase. Since the setup does not involve high currents running through the inductors for extended periods of time, the cooling times are reduced significantly, which enables quicker measurement campaigns.



(a) Inverted inductive UVRT test bench

(b) LC-resonant tank

(c) Grid simulator



(d) Series impedance with reactive power source

(e) Autotransformer switch-over

(f) Autotransformer switch-in

Figure 1: Principle circuit diagrams of the investigated OVRT test facilities

C. Grid simulator

A grid simulator comprises of an AC-amplifier with a programmable output voltage. A principle schematic is shown in figure 1c. A grid impedance can be realized either through emulation in the amplifier control (Hardware in the loop (HIL) system), through an output impedance of the amplifiers output transformer, or through a discrete series inductance between simulator and DUT. Thanks to the freely programmable voltage, the type of the possible faults only depends on the technical restrictions of the amplifier (max. output currents and voltages, dynamics of the the control, etc.). Grid simulators are available up to the multi-megawatt range. Some Simulators enable harmonic distortions within the control bandwidth, which can reach up to 10 kHz.

D. Series impedance with reactive power source

For this test setup, a controllable capacitive reactive power source is added in parallel to the DUT, as illustrated in figure 1d. Before the fault, the reactive power source is grid-synchronized, but operating in zero-power mode. Injecting a capacitive reactive power by the parallel source leads to a voltage drop over the line impedance, which causes the DUT voltage to rise. By returning to zero-power mode, the voltage returns to its nominal value. 3-phase, 2-phase and 1-phase faults can be generated by this setup. The working principle of this test setup can be compared to the behavior of a STATCOM. Since real-world faults show very transient voltage slopes, a sufficient high dynamic reactive power source is required for this approach.

E. Autotransformer switch-over

For this test setup, an autotransformer with suitable tappings for the desired voltage levels is used. This test bench requires at least two on-load circuit breakers to switch between the tappings (cf. see figure 1e). Before the fault, switch CB1 is closed and switch CB2 is opened, which results in nominal DUT voltage. Next, switch CB2 closes and CB1 opens in order to increase the DUT voltage to the desired value. Finally, by reversing the switch positions, the nominal voltage is provided again. This test setup enables 3-phase, 2-phase and 1-phase faults.

F. Autotransformer switch-in

For this test setup, an autotransformer with suitable tappings is used again. Unlike the autotransformer switch-over method, this approach only requires one circuit breaker, as displayed in figure 1f. Before the fault, the switch between the transformer and ground is open, which turns the upper windings of the transformer into a series inductance between grid and DUT. To produce an over-voltage situation, the circuit breaker is closed, leading to an OVRT event depending on the selected tapping. Even UVRT are possible, if the DUT can be connected to tappings in the lower part to the transformer (not shown in 1f). By opening the circuit breaker, the DUT voltage returns to its nominal value. This test setup enables again to test 3-phase, 2-phase and 1-phase faults [7], [8].

IV. Comparison of the transient behavior of test facilities

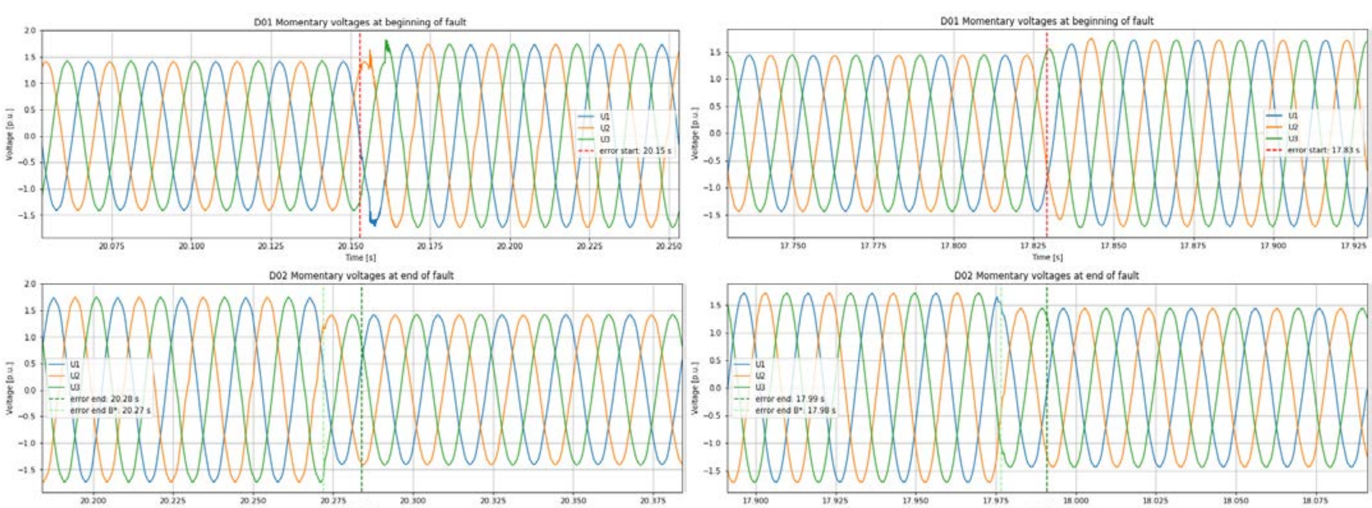
Due to the use of different technologies in the generation of over-voltage events, the transient behavior of the devices can vary greatly. Within the scope of this work, comparative measurements were carried out on all facilities in order to determine the behavior at the beginning and end of the fault. All tests were carried out as no-load tests. This means that no DUT was not connected to the test bench, which could influence the results by feeding or sinking any current from or to the test bench. The following factors were considered among others: The voltage slope and the over shoot at the fault start and end and the synchronicity of the voltage change on each phase.

A. Inverted inductive UVRT test bench

The beginning of the fault of this test bench is characterized by three individual arcing events, which are created when UVRT circuit breaker in each phases opens, as it can be observed in figure 2a. The opening event, in this case on a $20kV$ voltage level, produces an arc that will be cleared during the current's zero-crossing. Since the circuit is mainly inductive, this happens around the peak of the voltage. Besides this, voltage steps up to U_{OV} with a steep slope. For the end of the fault, this test bench is characterized by a fast step back to U_N without significant transient effects. In this case the voltage in all three phases react simultaneously, as can be seen in figure 2a.

B. LC-resonant tank

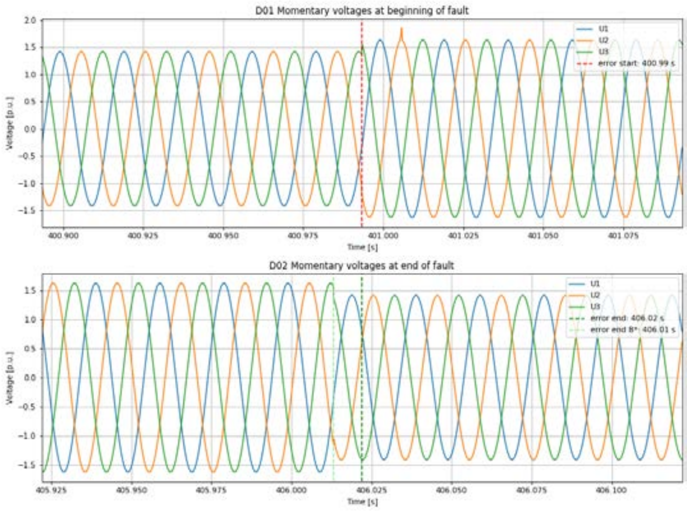
The beginning of the fault here is characterized by a voltage swell over a few milliseconds (up to on cycle), as can be seen in figure 2b. The reason for this is, that the charging process of the capacitors



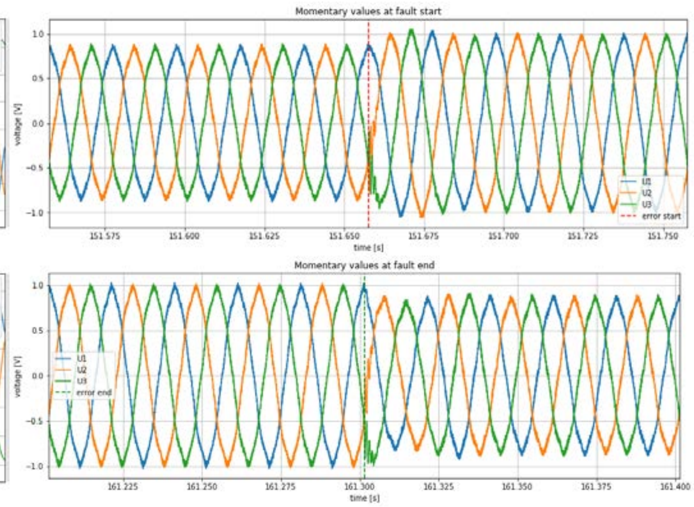
(a) Inverted inductive UVRT test bench

(b) LC-resonant tank

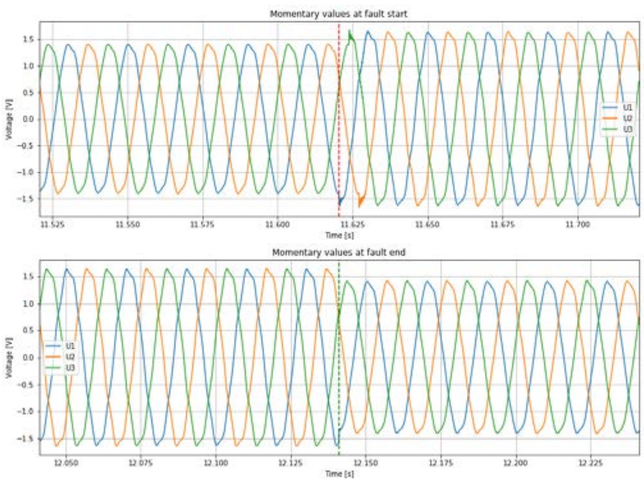
Figure 2: Transient behavior at the beginning and the end of the fault for the investigated OVRT test facilities



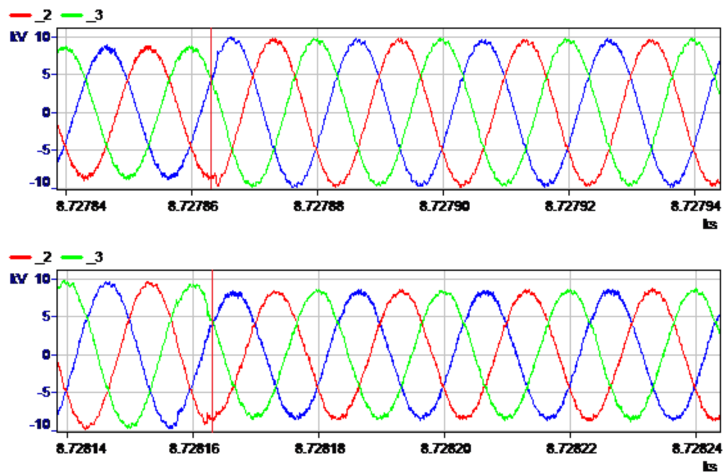
(a) Grid simulator



(b) Series impedance with reactive power source



(c) Autotransformer switch-over



(d) Autotransformer switch-in

Figure 3: Transient behavior at the beginning and the end of the fault for the investigated OVRT test facilities

from the pre-charged to U_N to the U_{OV} needs a given time, since the current is limited by the series choke. The end of the fault is again characterized by a fast step back to U_N without significant transient effects, as can be seen in figure 2b.

C. *Grid simulator*

For the grid simulator, the voltage swell can be freely programmed within the control bandwith of the amplifier, which here is $10kHz$. The beginning of the fault is plotted in figure 3a. Transient effects are usually not created by the simulator. Again, the free programmability enables a fast step back to U_N at the end of the fault without significant transient effects, as can be seen in figure 3a.

D. *Series impedance with reactive power source*

The voltage rise during the beginning of the fault, as shown in figure 3b, is characterized by two aspects: First, a oscillation can be witnessed on two phases, and second, the voltage shows a short overswing above the desired value, after which it settles to the final over-voltage value. This is probably due to the reactive power controller of the source, which should ideally be tweaked to better match real-world over-voltage events. The end of the fault is characterized by the same events in reverse: an oscillation and an under-shoot before settling back to nominal voltage.

E. Autotransformer switch-over

The beginning of the fault on this test bench shows a voltage swell, which is delayed by $60°$ between the phases, see figure 3c, due to arc clearing in the switch-over circuit. The end of the fault is, like with the other test benches, characterized by a fast step back to U_N without significant transient effects, as can be seen in figure 3c.

F. Autotransformer switch-in

The beginning and the end of the fault is depicted in Figure 3d. The beginning of the fault is characterized by a simultaneous voltage step in all three phases with a small transient over-shoots. The arc quenching effect in the circuit breakers lead to an non-simultaneous end of fault characteristic in the three phases. It should be mentioned, that the harmonic noise, which can be seen in Figure 3d, is not caused by the test equipment but by the weak grid connection point in this case.

V. Calculation of the impedance

To be able to investigate the change in impedances when a fault occurs, the impedances before and during the fault must be calculated. For the inverted UVRT and the LC resonant circuit the impedances can be determined via the inductors and capacitors used. The figure 1a shows that the impedance in the fault is given by the serial impedance in series with the grid impedance whereas before the fault, the UVRT inductor is additionally connected in parallel. For the LC resonant circuit, the impedance in case of a fault is given by the grid impedance with the series inductance and the parallel OVRT capacitor. The pre-fault impedance is determined by the OVRT capacitor and the grid impedance. For the test concept grid simulator no impedance changes result from the theoretical considerations. This can be justified by the behavior of the grid simulator, which does not change the output impedance when the voltage set point changes. The effective impedance is determined by the output characteristic of the grid simulator or by additionally inserted impedances between the DUT and the grid simulator. For the series impedance with reactive power source concept the impedance is determined by the grid, the reactive power source and the series impedances. The impedances for autotransformer switch-in concept can be calculated using the inductance of the transformer [8]. Depending on the desired over-voltage the corresponding transformer tab is used. The impedance from the DUT's point of view decreases in the fault compared to the pre-fault conditions. This applies equally to the UVRT and OVRT case.

VI. Evaluation of the test benches

In Table I three properties of the transient behavior at the fault start and fault end are listed. The voltage slope evaluates with which speed the voltage reaches the stationary over-voltage. Depending on the technique used, this happens immediately, the voltage jumps directly to the higher value or the voltage increases more slowly with a ramp. The synchronicity of the individual phases is examined. Do all phases react at the same time or are they shifted in time from one another. Overshooting can occur in different ways. Either on single phases (c.f. Figure 2a) or over a longer period of time on all three phases like in Figure 3b.

Table I: Evaluation of the test benches

Test bench	Voltage Slope at fault start/end	simultaneous phase reaction at fault start/end	over-/under-shoots or oscillations at fault start/end
A	Instantaneous	No/Yes	Moderate/No
B	Within 1 period	Yes/Yes	No/No
C	Instantaneous	Yes/Yes	No/No
D	Instantaneous	Yes/Yes	No/Moderate
E	Instantaneous	No/Yes	Moderate/No
F	Instantaneous	Yes/Yes	Moderate/No

VII. Conclusion and Outlook

In this paper six different concepts for generating a temporary over-voltage were presented. All test benches can be used for OVRT test, which are increasingly demanded in grid codes. The functionality of the respective test benches was presented and the transient behavior at the beginning and end of the fault were analyzed. It has been shown that there are significant differences in the principles. Four of the test benches use mechanical switches to achieve voltage increases by switching. Two others are based on power electronic amplifiers which generate the over-voltage event by changing between set points. The different technologies therefore show significant differences in transient behavior and the active impedances. Effects such as over-shoots, non-phase-synchronous changes in amplitudes, slow voltage ramps and immediate voltage changes can be observed. This different behavior of the test equipment may have an effect on the behavior of the tested devices.

In further work, tests under load with different DUTs will be performed and the influence of the test benches on the DUTs will be analyzed, too. Parameters such as the maximum voltage and the dynamic behavior can be determined. Realistic over-voltage scenarios will be defined and the realism of the test equipment should be evaluated. Using the calculated impedances, models of the test equipment can be created easily. In the further course of the project such models will be created and validated. Impedance characteristics of the test benches will be compared with the impedance behavior of real-world faults.

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